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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,001	10/25/2001	Schuyler E. Shimanek	X-969 US	9332

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EXAMINER	
TRAN, DENISE	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/040,001	SHIMANEK ET AL.	
	Examiner	Art Unit	
	Denise Tran	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *11-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-10,18-24 and 26-31* is/are rejected.

7)☒ Claim(s) *7 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/25/01,3/3/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-10 and 18-31, drawn to a method or apparatus, comprising: repeating, if the first detected value is different from a first stored value, transferring a first word from a non-volatile to the volatile memory, classified in class 365, subclass 189.07; 711/170 .

   II. Claims 11-17, drawn to an initialization circuit, comprising: a sensing array and a control circuit, classified in class 711, subclass 154; 365/230.05.

2. The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as in an apparatus lacked a sensing array and a control circuit. See MPEP § 806.05(d).

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. Because these inventions are distinct for the reasons given above and the search required for Group II is not required for Group I, restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Lois Cartier on 4/11/05 a provisional election was made with traverse to prosecute the invention of Group I, claims 1-10 and 18-31. Affirmation of this election must be made by applicant in replying to this Office action. Claims 11-17 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

6. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

7. Claims 1-10 and 18-31 are presented for examination.

8. Claims 7 and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-3, 5, 6, 8, 10, 18-21, 23, 24, 26-28, 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art, Applicant's specification pages 1-3 (hereinafter AAPA) in view of "Error Check and Correction for Soft Error of Random-Access Memory", IBM Tech. Disclosure, March 1989 (NN890358) (hereinafter IBM).

As per claims 1, 18, 19 and 31, AAPA shows the use of a method/apparatus of configuring a programmable logic device including non-volatile and volatile memories, the non-volatile memory including a plurality of words comprising configuration data for the programmable logic device, each word including a first transfer bit having a first stored value that is one of a "programmed" value and an "erased" value, the method/apparatus comprising:

powering up the programmable logic device (e.g. [0005]);

repeating the following sequence in response to the powering up for a series of the words in the non-volatile memory, from a first word to a final word: transferring one of the words from the non-volatile memory to the volatile memory (e.g. [0005]), and detecting a first detected value of the data transferred from the non-volatile memory to

the volatile memory (e.g. [0007-[0009]) and transferring the first word from the non-volatile memory to the volatile memory (e.g. [0005]).

AAPA does not specifically show the use of a first transfer bit and repeating, if the first detected value is different from the first stored value for any one word, transferring the first word from the non-volatile memory to the volatile memory. IBM shows the use of a first transfer bit (i.e., error flags) and when the first detected value is different from the first stored value for any one word (e.g. last paragraph), transferring the first word from the non-volatile memory to the volatile memory (i.e., the corrected data is stored back into memory as shown in IBM where it is subsequently read out as shown in AAPA) (e.g. last paragraph). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine IBM with AAPA because it would provide for a reduction in data errors.

As per claims 2 and 20, in addition to above AAPA shows the use of further comprising: beginning operation of the programmable logic device after the final word is successfully transferred (e.g. [0005] and detecting a first detected value of the data transferred from the non-volatile memory to the volatile memory (e.g. [0007]-[0009]). AAPA does not specifically show the use of if the first value for each word is the same as the first stored value for the same word. IBM shows the use of if the first value for each word is the same as the first stored value for the same word (e.g. last paragraph). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine IBM with AAPA because it would provide for a reduction in data

errors.

As per claims 3 and 21, AAPA shows the use of further comprising: storing the plurality of words in the non-volatile memory prior to powering up the programmable logic device (e.g. [0005].

As per claims 5 and 23, AAPA does not specifically show the use of wherein each word further includes a second transfer bit having a second stored value, the second stored value being different from the first stored value. IBM shows the use of each word further includes a second transfer bit (i.e., error flags) having a second stored value, the second stored value being different from the first stored value (i.e., error flags can be 0 or 1) (e.g. last paragraph). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine IBM with AAPA because it would provide for a reduction in data errors.

As per claims 6, 24, AAPA does not specifically show the use of for each transferred word, detecting a second detected value of the second transfer bit transferred from the non-volatile memory to the volatile memory; and repeating, if the second detected value is different from the second stored value for any one word, transferring the first word from the non-volatile memory to the volatile memory. IBM shows the use of a second transfer bit (i.e., error flags) and when the second detected value is different from the second stored value for any one word (e.g. last paragraph), transferring the first word from the non-volatile memory to the volatile memory (i.e., the

corrected data is stored back into memory as shown in IBM where it is subsequently read out as shown in AAPA) (e.g. last paragraph). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine IBM with AAPA because it would provide for a reduction in data errors.

As per claims 8, 26-28, AAPA shows the use of wherein the programmable logic device is a CPLD (e.g. [0005].

As per claims 10, 30, AAPA does not specifically show the use of wherein repeating transferring the first word is performed after detecting a first detected value and before transferring the final word. IBM shows the use of wherein repeating transferring the first word is performed after detecting a first detected value and before transferring the final word (e.g. last paragraph). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine IBM with AAPA because it would provide for quick detection and correction of any errors.

11. Claims 9 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art, Applicant's specification pages 1-3 (hereinafter AAPA) in view of "Error Check and Correction for Soft Error of Random-Access Memory", IBM Tech. Disclosure, March 1989 (NN890358) (hereinafter IBM) and in further view of "Official Notice".

As per claims 9 and 29, neither AAPA nor IBM shows the use of wherein repeating transferring the first word is performed only after transferring the final word.

"Official Notice" is taken that both the concept and advantages of providing for wherein repeating transferring the first word is performed only after transferring the final word is well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include wherein repeating transferring the first word is performed only after transferring the final word to the combined system of AAPA and IBM because it would provide for a reduction in bus usage. When each word is checked before another is sent, increases the amount of time the bus is being used. When all words are transferred and then checked, decreases the amount of time the bus is being used.

12. Claims 4 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art, Applicant's specification pages 1-3 (hereinafter AAPA) in view of "Error Check and Correction for Soft Error of Random-Access Memory", IBM Tech. Disclosure, March 1989 (NN890358) (hereinafter IBM) and in further view of Konigsburg, U.S. Patent No. 5,784,391.

As per claims 4 and 22, neither AAPA nor IBM show the use of wherein the first transfer bit is in the same location of each word. Konigsburg shows the use of wherein the first transfer bit is in the same location of each word (e.g. figure 2, field 18 (bits 129-136)). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine AAPA, IBM and Konigsburg because it would provide for easier and quicker access to the errors bits compared to having to search the data word for error bits.

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Lee et al. (5313425) shows a memory having an improved error correction capability;

b) Knefel (6539504) shows error monitoring system for multi bit errors;

c) Choi (6233717) shows checking and correcting data errors;

d) Maayan et al. (6584017) shows programming memory cell ;

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (571) 272-4189. The examiner can normally be reached on Monday, Thursday, and Friday from 8:45 a.m. to 5:15 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim, can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Denise Tran

4/28/05